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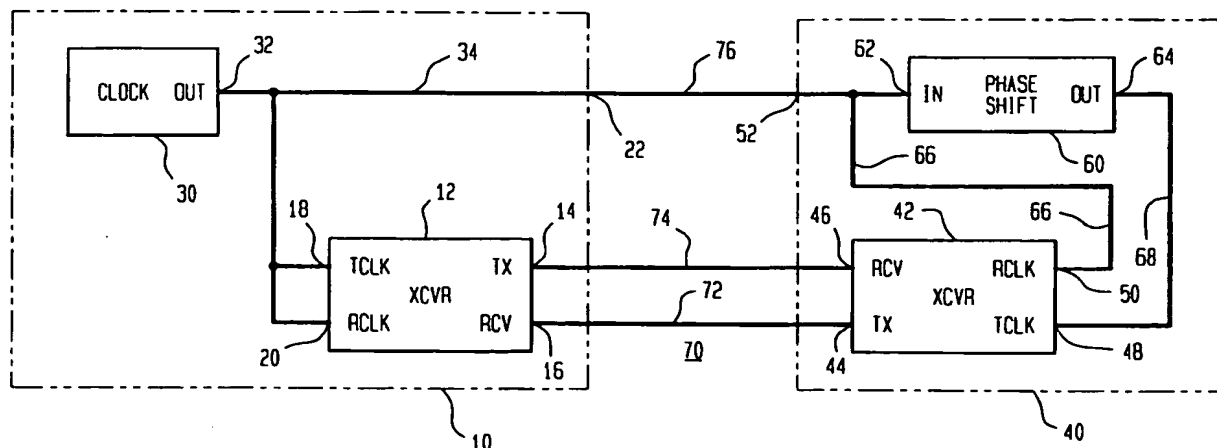
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(54) **Path delay compensation in an open-loop system.**

(57) One can compensate for signal propagation delay in an open-loop system of interconnected components by fixing the overall path propagation time

and selectively adjusting the transmit timing at each of the components.

FIG. 1**EP 0 603 600 A2**

Field of the Invention

This invention generally relates to the interconnection of units in a system. Specifically, the invention is directed to an apparatus and method for compensating for signal propagation delay in open-loop systems.

Background of the Invention

When dealing with two components interconnected in an open-loop system, one must provide a means of coordinating communications between the components. Some systems, for example, require that data from one component be received at another component at a specific point in time relative to a system clock. Because of the propagation delay experienced by the data in traveling between the components, one has to account for that delay on the receiving end. When the path delay is variable, such as where the length of an interconnecting cable varies, the accompanying variation in propagation time must be taken into consideration.

Summary of the Invention

These and other objects are achieved by a path delay compensation scheme that adjusts the time of transmission of data from one component in a system to another to cause data to arrive at that other component at a precise time relative to a local clock signal.

Brief Description of the Drawings

A more complete understanding of the present invention, as well as other objects and advantages thereof not enumerated herein, will become apparent upon consideration of the following detailed description and the accompanying drawings, wherein:

Figure 1 is a schematic block diagram of a system incorporating the invention;

Figure 2 is a schematic block diagram of the phase shift module;

Figure 3 is a schematic block diagram of the phase-locked loop circuit;

Figure 4 is a schematic block diagram of the variable clock-shift module;

Figure 5 is a schematic block diagram of the bit delay module; and

Figure 6 is a timing diagram showing the outputs of the multiplexer in the variable clock-shift module.

Detailed Description of the Invention

A block diagram of a communication system is shown in Figure 1. The system has two communications units, arbitrarily labeled local 10 and remote 40, interconnected by a communications path 70. Both the local unit 10 and the remote unit 40 each have a transmitter-receiver 12, 42. The transmitter-receivers 12, 42 each have a transmit port 14, 44, a receive port 16, 46, a transmit clock input 18, 48, and a receive clock input 20, 50.

The local unit 10 has three ports: the transmit port 14 and the receive port 16 of the transmitter-receiver 12, and a local clock port 22. A clock 30, having a clock output 32, provides a local clock signal on local timing line 34 to the transmit and receive clock inputs 18 and 20 of the transmitter-receiver 12. The clock signal output is also provided for transmission to the remote unit 40 at the local clock port 22.

The remote unit 40 also has three ports: the transmit port 44 and the receive port 46 of the transmitter-receiver 42, and a remote clock port 52. The remote unit 40 contains a phase shift module 60 having an input 62 and an output 64. The input 62 is connected to the remote clock port 52 by an input clock line 66 and the output 64 is connected to a remote timing line 68, which in turn provides transmit timing to the transmitter-receiver 42 through its transmit clock input 48. The input clock line 66 is also connected to the receive clock input 50 of the remote unit's 40 transmitter-receiver 42.

The local and remote units 10 and 40 are interconnected by a transmission path, in the case illustrated in Figure 1 the path being a cable 70. The cable 70 has two unidirectional transmission lines 72 and 74, which may carry data in serial, parallel, or some other form (digital, analog, etc.), and a unidirectional synchronization clock line 76. Line 72 interconnects the transmit port 44 in the remote unit 40 with the receive port 16 in the local unit 10. Similarly, line 74 interconnects the transmit port 14 in the local unit 10 with the receive port 46 in the remote unit 40.

The synchronization clock line 76, being connected between the local clock port 22 and the remote clock port 52, provides the remote unit 40 with the clock timing signal generated in the clock 30 of the local unit 10. The cable 70 could well have other lines but they are not illustrated here. Because a timing signal is not returned with the data, the system is characterized as open-loop.

As shown in Figure 2, the phase shift module 60 has a phase-locked loop 80 feeding a variable clock-shift module 82 through line 84. The phase-locked loop 80, shown in greater detail in Figure 3, has a comparator 90, a voltage-controlled oscillator 92, and a divide-by- n counter 94, interconnected

by lines 96, 98, and 100 as shown in the figure.

The variable clock-shift module 82 is shown in Figure 4. The module 82 essentially divides a clock signal of frequency nf into 2^d selectable pulses at a intervals over some period τ ($= a/nf$), where $a \geq d$, each of which has a different phase relationship with respect to each other. The input (line 84) to the module 82 is connected to a divide-by- a counter 110 having b outputs, Q_1 through Q_b , where $b \geq \log_2 a$ in a binary system. These b outputs are connected by lines 112 to corresponding inputs 1 through b of a b -to- c decoder 114. The outputs 1 through c of the decoder 114 are connected in turn by lines 116 to inputs 1 through 2^d of a 2^d -to-1 multiplexer 118, respectively.

The multiplexer 118 is enabled by select lines 122 connected to select inputs S_1 through S_d , and its output is connected to the D input of a D-type flip-flop 124. The clock signal is provided on a clock input line 126 tied to line 84. The output 64 of the module 82 is the Q output of the flip-flop 124. An example of the selectable outputs MUX1-MUX8 of the multiplexer 118 is illustrated by the timing diagram in Figure 6, which assumes a division-by-8 of the clock signal on line 84.

For simplicity of presentation, there is a one-to-one correspondence between the respective interconnections of the counter 110, the decoder 114, and the multiplexer 118. However, it should be understood that this is not required and one may choose to omit and/or transpose selected connections to suit individual design needs.

An additional module, not shown in the overall block diagrams of Figures 1 and 2, is the bit-shifting module 140. This component can be inserted at the transmit port 44 of the transmitter-receiver 42 in the remote unit 40. However, one could place this module 140 on either side of the port 44. The purpose of the bit-shifting module 140 is to adjust the time of transmission of the data in some selected number of whole-bit increments, as determined by the user.

As shown in Figure 5, the bit-shifting module 140 is a series of p cascaded D-type flip-flops 142, having a data input 148 connected to the D input of the first flip-flop FF1 142. The Q output of every flip-flop 142 but the last is tied to the D input of the next device. The clock input is derived from the output of the phase shift module 60 on line 68. The data input 148 and the Q outputs of the flip-flops are also provided by lines 152 as inputs to a q -to-1 multiplexer 144, where $q = p + 1$. The multiplexer 144 is enabled by z select lines 146 connected to select inputs S_1 through S_z , to provide an output 150.

Operation of the System

Consider bidirectional communications between the local and remote units 10 and 40. The local unit 10 transmits data along line 74 to the remote unit along with a synchronizing clock signal on line 76. When the data arrives at the transmitter-receiver 42 in the remote unit 40, it is clocked in by the received clock signal applied to receive clock port 50.

To send data from the remote unit 40 to the local unit 10, the timing must now be coordinated as the local unit 10 will be looking for the data at a precise point in time T_D relative to the synchronizing signal (line 34) at the receive clock input 20. This represents the total round trip delay from the local unit 10 to the remote unit 40 and back again.

To achieve a transfer within this period of time, one must account for the propagation delay time of the cable (T_C each way) and the propagation delay of the electronics of the remote unit 40 (D_E). Given that a round trip entails passage of the synchronizing clock signal through the cable 70 to the remote unit 40, and then passage of the data through the remote unit 40 and onto and through the cable 70 to the local unit 10, the total delay time T_D will be $2 \cdot T_C + D_E$. The quantity T_D is selected to allow for the largest required round trip transit time.

Since changes in path delay between the units 10 and 40 (denoted as T_C') will result in variations in total propagation time, a variable quantity T_S is utilized to achieve a constant T_D , where:

$$2 \cdot T_C' + D_E + T_S = T_D \quad (1)$$

The time interval T_S represents the shift in time of the data that must occur in the remote unit 40 so that the data is received at the local unit in an elapsed time of T_D .

The time shift T_S would have possibly one, two, or more components. The first component is T_{Si} , the fractional bit time shift. Depending on the desired granularity, one could shift the timing of the transmit clock signal at transmit clock input 48 in the remote unit 40 by some fractional portion of one bit length, as illustrated in Figure 6 using the circuit of Figure 4, effectively time shifting the data an equivalent amount.

The second component is T_{Sb} , the whole bit time shift of the data (Figure 5). This affords a time shift greater than T_{Si} . If desired, one could achieve a greater delay by shifting larger units, such as a byte of data. Therefore, the total shift T_S would be the sum of T_{Si} , T_{Sb} , and perhaps a further component. Given that

$$T_D = 2 \cdot T_C' + D_E + T_S \quad (2)$$

and, assuming only two components of shift:

$$T_D = 2 \cdot T_C' + D_E + T_{SI} + T_{SB} \quad (3)$$

Since T_D and D_E are fixed numbers, and the value of T_C' is determined by the path delay through the cable, one can thus calculate T_{SI} and, if need be, T_{SB} . In most applications, insertion of the T_{SI} component will be sufficient. Where a greater delay is desired, one may have to resort to T_{SB} . Therefore:

$$T_{SI} + T_{SB} = T_D - (2 \cdot T_C' + D_E) \quad (4)$$

The exact values of T_{SI} and T_{SB} are set by enabling the select lines 122 and 146 of the 2^d-to-1 multiplexer 118 and the g-to-1 multiplexer 144, respectively. To perform the selection in the outputs of the multiplexers 118 and 144, the appropriate select lines 122 and 146 would be connected to ground or V_{CC} , as required. It should be understood that one could use T_{SB} independently of T_{SI} if whole-bit manipulation would provide sufficient resolution. Moreover, if no shift is desired, one could select either an unshifted multiplexer output signal (MUX1 in Figure 6) or the signal on the input clock line 66. The latter could be provided directly to the transmit clock input 48, bypassing the phase shift module 60.

It should also be understood that the local and remote clocks may differ in frequency and duty cycle as required by the particular implementation. Also, the transmit data rates and the synchronization clock frequency may differ. Moreover, this scheme can be used with systems having more than two components. For example, where there are three or more communications modules connected in a system, the same method of adjusting the transmit time relative to a clock at the ultimate destination will serve to insure that data arrives at the receiving module at the proper time.

While there has been described what is believed to be the preferred embodiment of the invention, those skilled in the art will recognize that other and further modifications may be made thereto without departing from the spirit of the invention, and it is intended to claim all such embodiments that fall within the true scope of the invention. For example, this method could also have other applications such as compensating for delay over a wireless path (e.g., such as a microwave link), where the distance changes depending on the application. Also, the techniques here are not limited to digital data, but may encompass analog signals as well.

Claims

1. An apparatus, comprising:
 - means for receiving a synchronizing timing signal;
 - means, responsive to the synchronizing timing signal, for transmitting data; and
 - means for selectively adjusting the time of transmitting.
2. An apparatus as set forth in claim 1, wherein the means for selectively adjusting includes:
 - means for deriving an intermediate signal from the synchronizing timing signal; and
 - means for adjusting the phase of the intermediate timing signal.
3. An apparatus as set forth in claim 1, wherein the means for selectively adjusting includes:
 - means for deriving at least one intermediate signal from the synchronizing timing signal, where each intermediate signal has a unique phase relationship with respect to the synchronizing timing signal; and
 - means for selecting either an intermediate signal or the synchronizing timing signal.
4. An apparatus as set forth in claim 1, wherein the means for selectively adjusting includes means for delaying the data in whole-number time intervals of the data.
5. An apparatus as set forth in claim 1, wherein the means for selectively adjusting includes means for delaying the data in fractional-number time intervals of the data.
6. An apparatus for compensating for delay over a transmission path from a first point to a second point, comprising:
 - means for receiving a synchronizing timing signal transmitted over the path from the first point to the second point;
 - means, responsive to the synchronizing timing signal, for transmitting data over the path from the second point to the first point; and
 - means for selectively adjusting the time of transmitting.
7. A method of timing, comprising the steps of:
 - receiving a synchronizing timing signal;
 - in response to the synchronizing timing signal, transmitting data; and
 - selectively adjusting the time of transmitting.

8. A method as set forth in claim 7, wherein the step of selectively adjusting includes the steps of:
deriving an intermediate signal from the synchronizing timing signal; and
adjusting the phase of the intermediate timing signal. 5
9. A method as set forth in claim 7, wherein the step of selectively adjusting includes the steps of:
deriving at least one intermediate signal from the synchronizing timing signal, where each intermediate signal has a unique phase relationship with respect to the synchronizing timing signal; and
selecting either an intermediate signal or the synchronizing timing signal. 10 15
10. A method as set forth in claim 7, wherein the step of selectively adjusting includes the step of delaying the data in whole-number time intervals of the data. 20
11. A method as set forth in claim 7, wherein the step of selectively adjusting includes the step of delaying the data in fractional-number time intervals of the data. 25
12. A method of compensating for delay over a transmission path from a first point to a second point, comprising the steps of:
receiving a synchronizing timing signal transmitted over the path from the first point to the second point;
in response to the synchronizing timing signal, transmitting data over the path from the second point to the first point; and
selectively adjusting the time of transmitting. 30 35 40

45

50

55

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FIG. 1

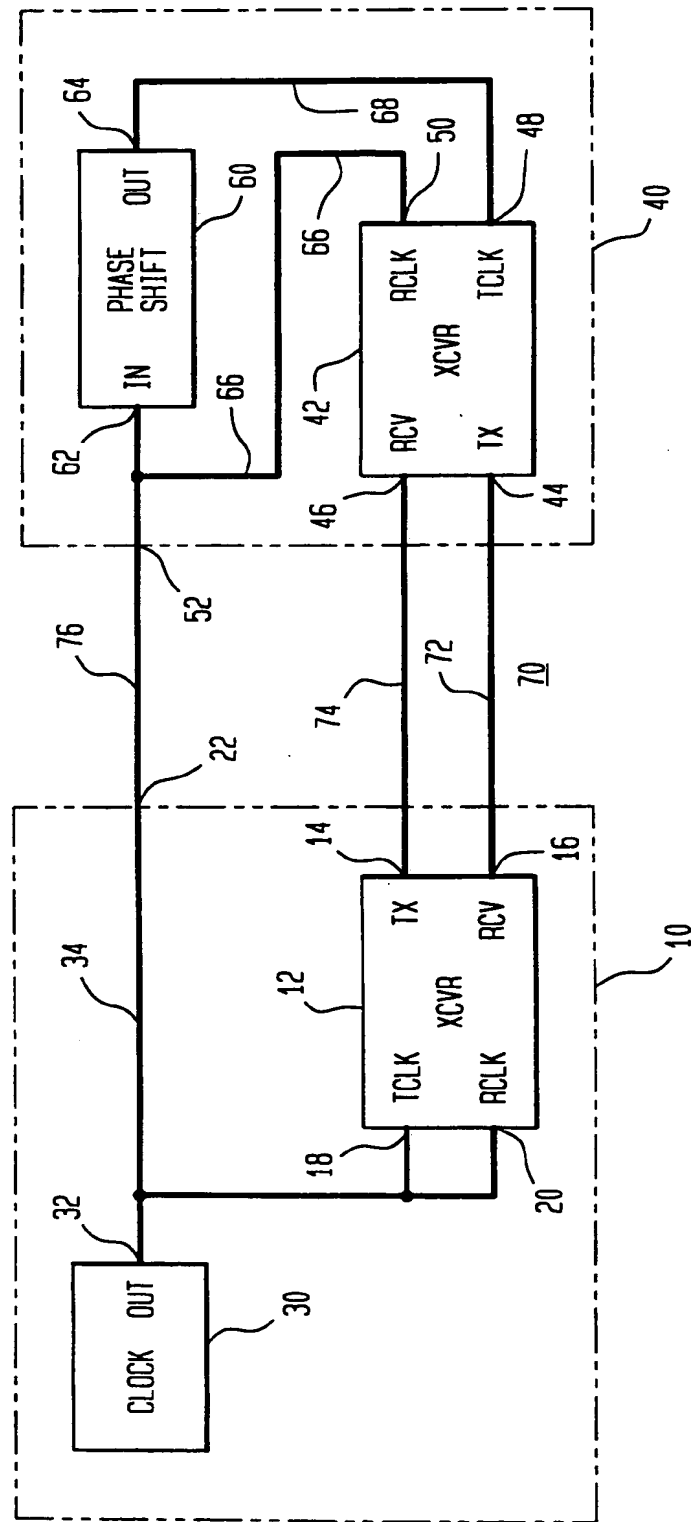


FIG. 2

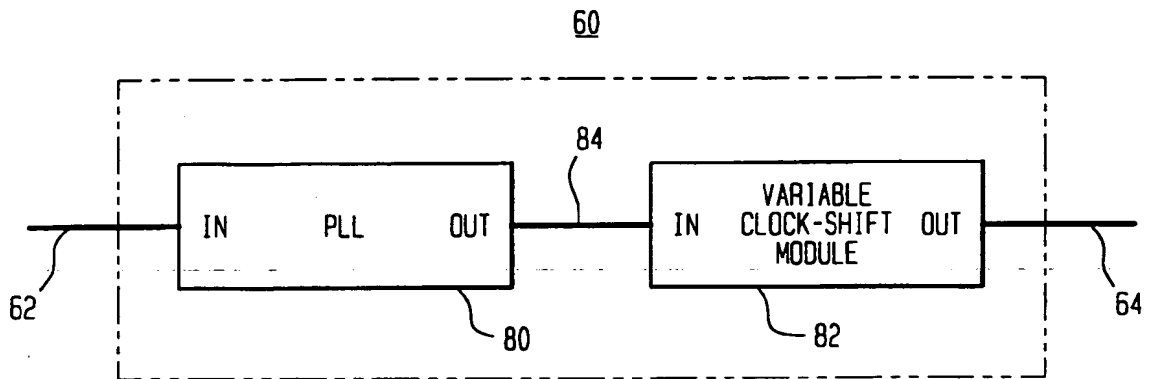


FIG. 3

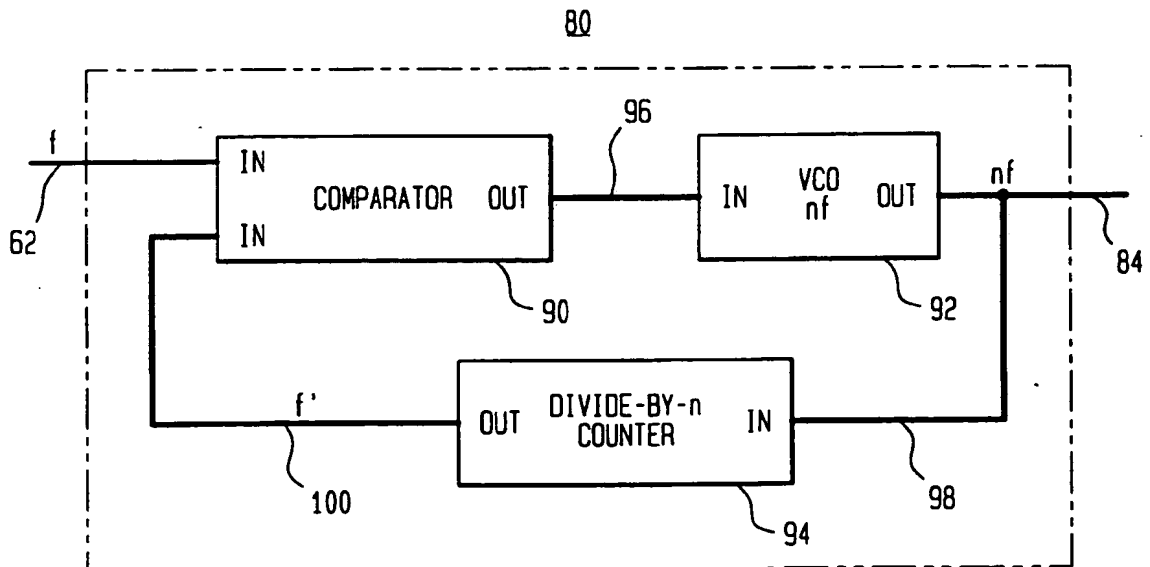


FIG. 4

82

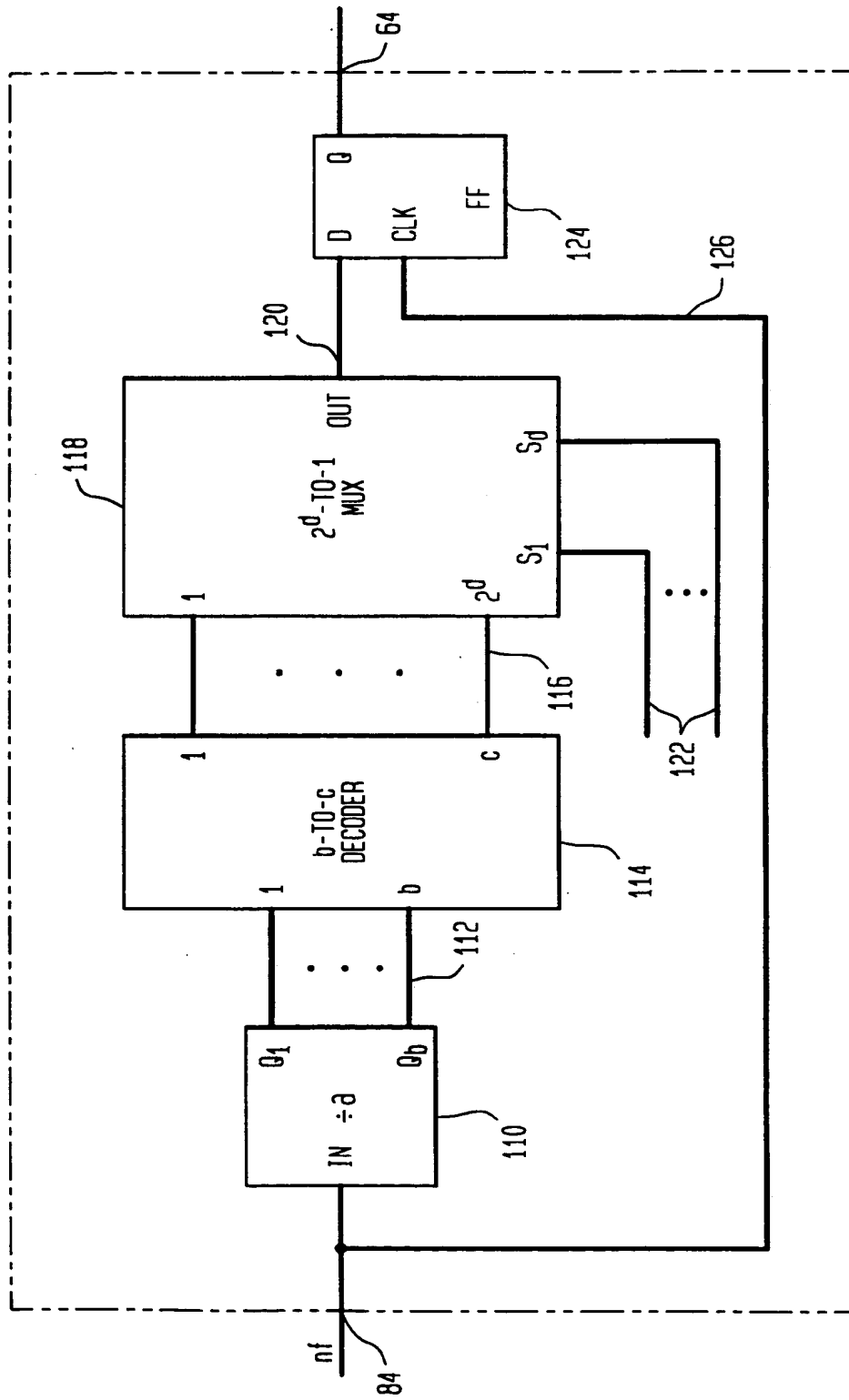


FIG. 5

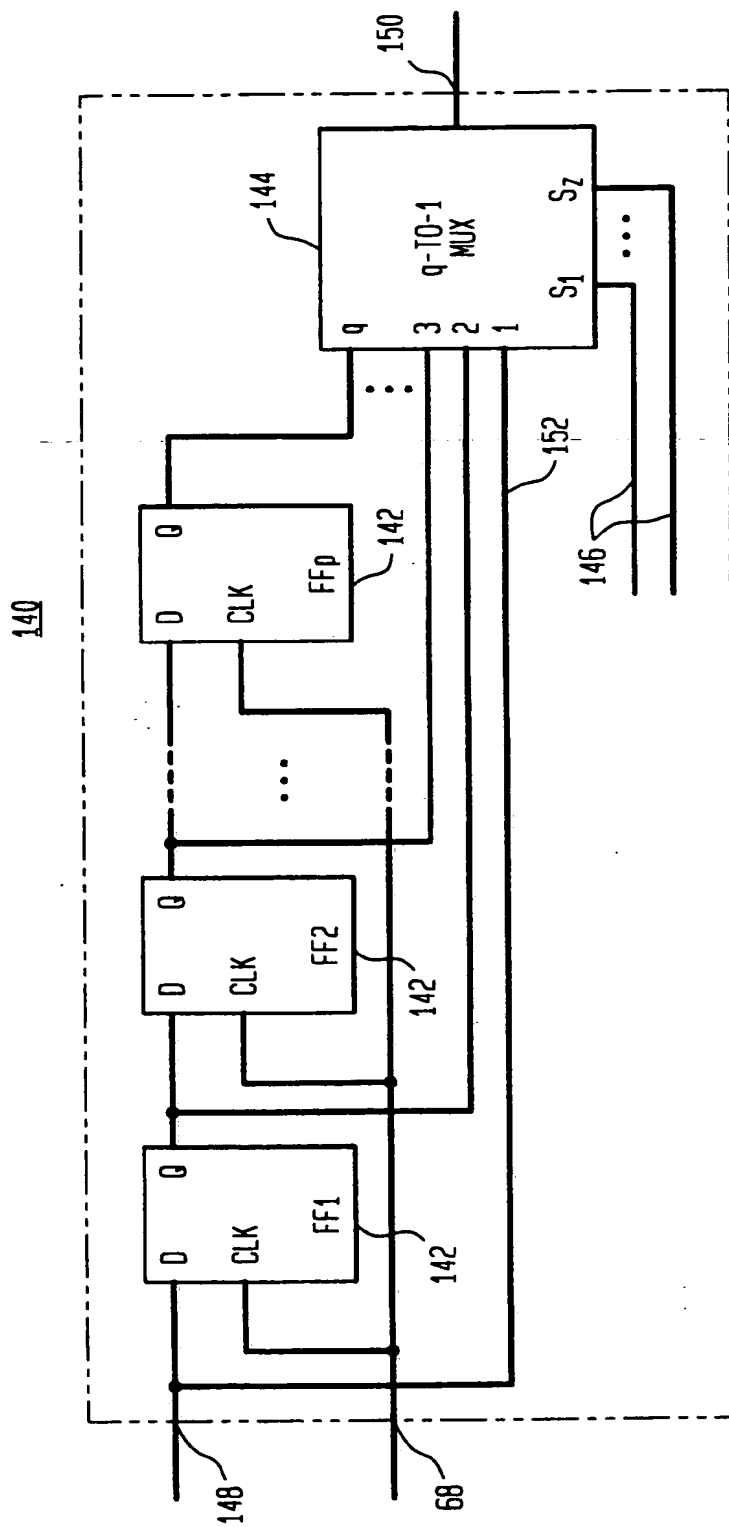


FIG. 6

